CLAIMS

What is claimed is:

1. A multi-channel detector readout apparatus, comprising:

(a) means for selecting a channel for output from a plurality of detector input channels carrying corresponding input signals having amplitudes, wherein said selected channel comprises the detector input channel having a signal amplitude exceeding a threshold level and further exceeding the amplitude of the signals on the remaining input channels during a sample period; and

(b) a circuit providing said means for selecting said channel.

2. An apparatus as recited in claim 1, wherein said circuit comprises an input sampling stage configured for outputting signal samples to a sensing stage, said sensing stage configured for comparing the amplitudes of said signal samples with said threshold level and for comparing the amplitudes of said signal samples with each other.

3. A multi-channel detector readout circuit, comprising:

(a) a multiplexer stage having a plurality of inputs and an output, said multiplexer configured for receiving a plurality of analog input signals, said multiplexer configured for receiving a multiplexer selection signal directing which of the plurality of input signals is to be routed to the output;

(b) an amplitude sensing stage having a noise floor threshold circuit, said

amplitude sensing stage configured for receiving a plurality of analog input signals and selecting the analog input signal having an amplitude which exceeds a noise floor threshold and having the highest signal amplitude, said amplitude sensing stage configured for outputting a channel identification corresponding to said selected input signal; and

(c) a digital control section configured for receiving said channel identification and controlling said multiplexer stage to pass an input signal from said selected channel to said output.

4. A multi-channel detector readout circuit as recited in claim 3, further comprising an analog channel masking stage capable of masking out selected inputs to said amplitude sensing stage in response to a control signal from said digital control section.

5. A multi-channel detector readout circuit as recited in claim 3, further comprising conditioning circuitry for shaping said analog input signals prior receipt by said multiplexer stage.

6. A multi-channel detector readout circuit as recited in claim 5, wherein said conditioning circuitry includes a controllable amplification stage for amplifying said analog input signals, said controllable amplification stage being controlled by a control signal received therein from said digital control section.

7. A multi-channel detector readout circuit as recited in claim 5, wherein the conditioning circuitry for each channel includes a sample and hold circuit for retaining the signal level of said analog input signal from a given sample is taken until the following sample is taken.

8. A multi-channel detector readout circuit as recited in claim 7, further comprising a digital noise suppression circuit which is capable of holding portions of said digital control section in a substantially static mode during time periods when said sample is taken so that reduced levels of digital noise are generated and coupled into said sample and hold circuitry and said multiplexer stage.

9. A multi-channel detector readout circuit as recited in claim 3, wherein the multiplexer receives sixty-four channels of the analog input signals from a detector.

10. A multi-channel detector readout circuit as recited in claim 3, further comprising a digital interface within the digital control section to allow external manipulation of internal integrated circuit operation and modes.

11. A multi-channel detector readout circuit as recited in claim 10, wherein commands are communicated on the digital interface in serial format.

12. A multi-channel detector readout circuit as recited in claim 10, wherein commands received from the digital interface on the digital control section are capable of selectably engaging multiple modes of device operation comprising:

(a) a channel gain mode in which the input channel gain is capable of being set in accord with commands on the digital interface;

(b) a user multiplexer mode in which output is selected from the multiplexer stage in accord with commands on the digital interface; and

(c) a winner-take-all mode in which the output of the amplitude sensing stage drives selection within said multiplexer stage.

13. A multi-channel detector readout circuit as recited in claim 12, further comprising a masking mode wherein inputs to the amplitude sensing stage are capable of being selectively masked so as not to participate in the signal selection process.

14. A multi-channel detector readout circuit as recited in claim 12, further comprising a test mode wherein functional aspects of internal circuits are tested by the injection of test signals on the input lines of said multi-channel detector.

15. A multi-channel detector readout circuit as recited in claim 3, wherein the multi-channel detector readout circuit is included within a single integrated circuit device.

16. A multi-channel detector readout device capable of receiving input signals from a plurality of detectors connected to the inputs of sample and hold circuits whose outputs are connected to a multiplexer and an amplitude sensing circuit which provides a digital line select output corresponding to the input signal with having the highest amplitude, the digital line select output signal being received by the multiplexer which routes a signal homologous with the highest amplitude signal to its singular output, wherein the improvement comprises:

(a) a noise floor threshold circuit that operates in conjunction with the amplitude sensing circuit to restrict input signal selection to those input signals which exceed a signal threshold as provided by a reference signal.

17. A multi-channel detector readout device as recited in claim 16, further comprising a digital control section interceding between said amplitude sensing circuit and said multiplexer such that the digital outputs from the amplitude sensing circuit are received by said digital control section, and said digital control section is capable of controlling said multiplexer to pass either a signal corresponding with said digital line select output from the amplitude sensing circuit or from a particular input signal, as selected by a command received within the digital control section.

18. A multi-channel detector readout device as recited in claim 17, further comprising a controllable amplification stage preceding the sample and hold circuits for amplifying the input signals, the controllable amplification stage being controlled by

signals received therein from said digital control section.

19. A multi-channel detector readout device as recited in claim 18, further comprising a controllable resistance reset device connected between the input and output of the controllable amplification stage to provide compensation of channel to channel differences in background amplitude.

20. A multi-channel detector readout device as recited in claim 18, further comprising a channel masking circuit capable of masking selected input signals to the amplitude sensing circuit under the direction of said digital control section.

21. A multi-channel detector readout circuit as recited in claim 16, further comprising a test circuit input connected to the individual inputs of said sample and hold circuits to provide for the testing of said multi-channel detector readout circuit without disconnecting input signals connected thereto.

22. A multi-channel detector readout circuit as recited in claim 21, further comprising a switch which is connected between said test circuit input and said sample and hold circuits, and is capable of controlling test signal receipt by said sample and hold circuits.

23. An integrated circuit providing multi-channel detection and identification of a highest amplitude signal, comprising:

(a) conditioning circuitry which shapes the signals on a plurality of analog input lines;

(b) sample and hold circuitry which samples the analog input lines to provide sampled analog signals;

(c) signal selection circuitry receiving a plurality of sampled analog signals and producing a single analog signal output, said signal selection circuitry additionally receiving signals that direct which of the plurality of sampled analog signals are to be routed to the analog signal output;

(d) signal identification circuitry having a noise floor threshold circuit, said signal identification circuitry receiving sampled analog signals and sensing which, if any, of these sampled analog signals meet a selection criterion which includes exceeding a noise floor threshold amplitude and having the highest amplitude within the aggregation of sampled analog signals, said signal identification circuitry capable of generating a line number which identifies the sampled analog signal which met the selection criterion; and

(e) digital control circuitry receiving said line number and capable of directing the signal selection circuitry to pass the sampled analog signal associated with said line number to said output signal line.

24. An integrated circuit as recited in claim 23, wherein the conditioning circuitry includes an amplification stage under the control of the digital control section which is capable of amplifying signal from the analog input lines.

25. An integrated circuit as recited in claim 23, wherein at least a portion of the circuitry within the multi-channel detection integrated circuit is held at least partially static during time intervals synchronized with taking of samples from the analog input lines so as to reduce the amount of digital noise which is coupled into the analog circuitry of the multi-channel detector integrated circuit.

26. An integrated circuit as recited in claim 23, further comprising a digital interface within the digital control section to allow external manipulation of internal integrated circuit operation and modes.

27. An integrated circuit as recited in claim 26, wherein commands received from the digital interface on the digital control section are capable of selectably engaging modes of device operation, comprising:

(a) a channel gain mode in which input channel gain is capable of being selected;

(b) a user multiplexer mode in which selection of the sampled analog signal to be output by the multiplexer is performed; and

(c) a winner-take-all mode in which the output of the signal identification

circuitry can be selected to drive channel selection within the signal selection circuitry.

28. An integrated circuit as recited in claim 27, further comprising a masking mode wherein inputs to the signal identification circuitry are capable of being selectively masked so as not to participate in the signal selection process.

29. An integrated circuit as recited in claim 27, further comprising a test mode wherein functional aspects of internal circuits within the multi-channel detection integrated are tested by the injection of test signals into the analog input lines.

30. A circuit for selecting a maximum amplitude signal from a plurality of detector inputs, comprising:

(a) a conditioning stage which shapes the analog signals on a plurality of analog input lines and includes selectable amplification of the analog signals;

(b) a sample and hold stage which provides for sampling of the analog input lines to provide sampled analog signals;

(c) a signal selection circuit capable of receiving a plurality of sampled analog signals and of producing a single analog output, said signal selection circuit additionally receiving signals that direct which of the plurality of sampled analog signals is to be routed to the analog output;

(d) a masking stage receiving sampled analog signals from said sample and hold stage and capable of selectably masking out any of said sampled analog signals;

(e) a signal identification circuit having a noise floor threshold circuit, and receiving a plurality of sampled analog signals from said masking stage, said signal identification circuit capable of sensing which sampled analog signal meets a selection criterion which includes exceeding a noise floor threshold and having the highest amplitude of all the sampled analog signals, said signal identification circuit thereafter outputting a line number corresponding to the sampled analog signal which meets the selection criterion; and

(f) a digital control section capable of controlling said selectable amplification, said masking stage, and said signal selection circuit, the digital control section further capable of receiving and selectably passing said line number to the signal selection circuit for controlling the selection of which sampled analog signal is to be output by said signal selection circuit.

31. A method of identifying a maximum amplitude input within a plurality of inputs, comprising:

(a) receiving a plurality of input lines;

(b) comparing the signal amplitude on each input line in comparison with a predetermined noise threshold;

(c) comparing the signal amplitude on each input line in comparison with one-another;

(d) outputting a digital channel selection signal which identifies an input line that both exceeds the predetermined noise threshold and the amplitude of the other

input lines; and

(e) selecting the identified input line in response to the digital channel selection signal and selectively passing a signal which corresponds to the signal amplitude of the identified input line to an output.

32. A method as recited in claim 31, further comprising selectively amplifying the input lines prior to comparing the signal amplitudes on the input lines with the predetermined noise threshold.

33. A method as recited in claim 32, further comprising noise stabilizing the digital section by entry into a reduced operation mode for the digital circuitry during sampling so as to reduce the digital noise coupled into each analog sample.

34. A method as recited in claim 31, further comprising selectively amplifying the input lines prior to comparing the signal amplitudes of the input lines with the predetermined noise threshold.